GOC-BF440-P

Bluetooth+WIFI Module Hardware Specification

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Be careful:

1. The module must use ladder steel net, and recommend ladder steel net thickness 0.16--0.20mm. The adaptability of the products is adjusted accordingly.

2. Before the use of the module, bake at 60 degrees centigrade and bake for 12 hours.

Release Record

Version Number	Release Date	Comments
V1.0	2018/08/31	Initial draft
V1.1	2019/07/03	Increase the power on time sequence Modification PCB Layout Footprint
V1.2	2019/07/23	Increase packing methods and performance parameters
V1.3	2019/08/08	Cancel reference design
V1.4	2019/08/19	Increase module height
V1.5	2020/01/06	Update Introduction

Contents

1. Introduction

The GOC-BF440-P device provides the highest level of integration for Automotive IoT wireless systems with integrated single-stream IEEE 802.11a/b/g/n/ac MAC/baseband/radio and Bluetooth 5.0 (Basic Rate, Enhanced Data Rate and Bluetooth Low Energy).

The GOC-BF440-P(CYW88373) brings the latest mobile connectivity technology for Automotive Infotainment, Telematics and rear-seat Entertainment.It also offers Automotive Grade 3 (–40 ℃ to +85 ℃) temperature performance, which is tested to AEC-Q100 environmental stress guidelines.

GOC-BF440-P supports all rates specified in the IEEE 802.11 a/b/g/n/ac specifications. IEEE 802.11ac's 256 QAM is supported for MCS8 in 20 MHz channels and MCS8/MCS9 in 40 MHz & 80 MHz channels to enable data rates of up to 433.3 Mbps. Included on-chip are 2.4 GHz and 5 GHz power amplifiers and low-noise amplifiers. Optional external PAs and LNAs are also supported.

The WLAN section supports the following host interface options: an PCIe Gen1 (3.0 compliant) interface. The Bluetooth section supports high-speed 4-wire UART interface.

The GOC-BF440-P implements highly sophisticated enhanced collaborative coexistence hardware mechanisms and algorithms, which ensure that WLAN and Bluetooth collaboration is optimized for maximum performance. In addition, coexistence support for external radios (such as LTE cellular) is provided via an external interface.

2. Block Diagram

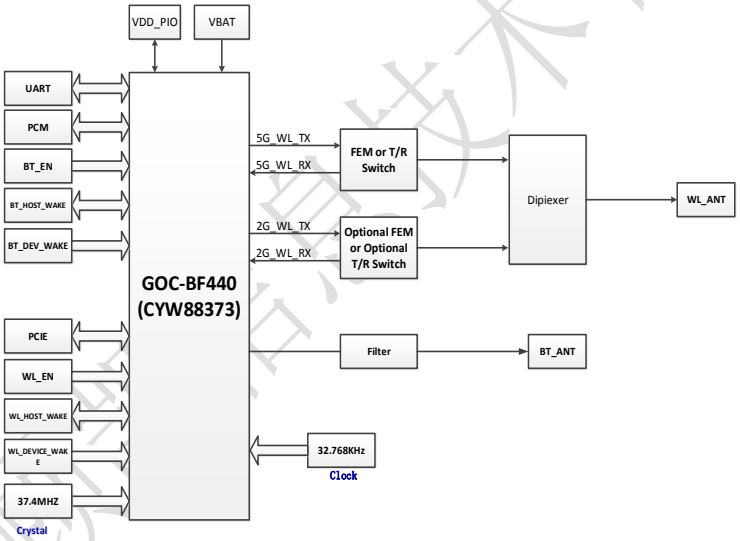


Figure 1: GOC-BF440-P System Block Diagram

3.Features

3.1 WIFI Features

IEEE 802.11ac compliant.

- Support for MCS8 VHT20 in 20 MHz channels for up to 86.7Mbps data.
- Single-stream spatial multiplexing up to 433.3 Mbps data rate.
- Supports 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation).
- Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- On-chip power amplifiers and low-noise amplifiers for both bands.
- Support for optional front-end modules (FEM) with external PAs and LNAs.

■ Supports integrated T/R switch for 2.4 GHz band.

■ Supports RF front-end architecture with a single dual-band antenna shared between Bluetooth and WLAN for lowest system cost.

■ Shared Bluetooth and WLAN receive signal path eliminates the need for an external power splitter while maintaining excellent sensitivity for both Bluetooth and WLAN.

■ Supports IEEE 802.15.2 external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE.

3.2 Bluetooth Features

- Bluetooth 5.0 qualified with all errata (applicable to v4.2 and earlier) fixed as well as all support for all optional Bluetooth 4.2 features
- Fully supports Bluetooth Core Specification version 5.0 + EDR features:
  - Adaptive frequency hopping (AFH)
  - Quality of service (QoS)
  - Extended synchronous connections (eSCO)—voice connections
  - Fast connect (interlaced page and inquiry scans)
  - Secure simple pairing (SSP)
  - Sniff subrating (SSR)
  - Encryption pause resume (EPR)
  - Extended inquiry response (EIR)
  - Link supervision timeout (LST)
- UART baud rates up to 4 Mbps
- Supports all Bluetooth 5.0 + HS packet types
- Supports maximum Bluetooth data rates over HCI UART
  - Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Trigger Cypress fast connect (TCFC)
- Narrow band and wide band packet loss concealment
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling
- Channel quality driven data rate and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features

3.3 Standards Compliance

- Bluetooth
  - Bluetooth 2.1 + EDR
  - Bluetooth 3.0
  - Bluetooth 4.2 Bluetooth Low Energy
  - Bluetooth 5.0
- IEEE 802.11 WLAN
  - IEEE 802.11ac Enhancements for Very High Throughput for Operation in Bands below 6 GHz
  - IEEE 802.11n Enhancements for Higher Throughput
  - IEEE 802.11a High-speed Physical Layer in the 5 GHz Band
  - IEEE 802.11b Higher-Speed Physical Layer Extension in the 2.4 GHz Band
  - IEEE 802.11g Further Higher Data Rate Extension in the 2.4 GHz Band

- IEEE 802.11d Specification for operation in additional regulatory domains
- IEEE 802.11r Fast Basic Service Set (BSS) Transition
- IEEE 802.11w Protected Management Frames
- IEEE 802.11e Medium Access Control (MAC) Quality of Service Enhancements
- IEEE 802.11h Spectrum and Transmit Power Management Extensions in the 5 GHz band
- IEEE 802.11i Medium Access Control (MAC) Security Enhancements
- IEEE 802.11k Radio Resource Measurement of Wireless LANs

- IEEE 802.15.2 Coexistence Compliance (on-silicon solution compliant with IEEE 3-wire requirements)
- WLAN Security:
  - WEP
  - WPA-Personal
  - WPA2-Personal
  - AES (hardware accelerator)
  - TKIP (hardware accelerator)
- Wi-Fi Multimedia:
  - WMM
  - Wi-Fi Multimedia - PowerSave (WMM-PS with U-APSD)
  - WMM-Sequential Access (WMM-SA with PCF)

4. Specification

Feature	Description
Model Name	GOC-BF440-P
Bluetooth	
Bluetooth Standard	Bluetooth V5.0
Frequency Band	2402MHz~2480MHz
Interface	UART/PCM
WIFI	
Frequency Band	2.4GHz/5GHz
Interface	PCIE
EVM	IEEE 802.11b;BPSK-1M@-13 dB QPSK-11M @-13dB IEEE 802.11g: BPSK-6M@-5 dB 64QAM -54M@-25dB IEEE 802.11n: BPSK- MCS0@-5 dB 64QAM -MCS7@-28dB IEEE 802.11a: BPSK-6M@-5dB 64QAM -54M@-25dB IEEE 802.11n: BPSK-MCS0@-5dB 64QAM - MCS7@-28dB IEEE 802.11ac: BPSK-MCS0@-5dB 256QAM – MCS8@-30dB 256QAM – MCS9@-32dB
Sensitivity@PER	802.11b:11M/-88dBm@<8%PER 802.11g:54M/-75dBm@<10%PER 802.11n:HT20-MCS7/-73dBm@<10%PER 802.11a:54M/-72dBm@<10%PER 802.11n:HT20-MCS7/-70dBm@<10%PER HT40M- MCS7/-67dBm@<10%PER 802.11ac: HT20 MCS9/-64dBm@<10%PER HT40M-MCS9/-61dBm@<10%PER (Tolerance:+/-1dB)

RF Power	802.11b/11M: 17dBm+/-1dBm 802.11g/54M: 16dBm+/-1dBm 802.11n/HT 20- MCS7: 14dBm+/-1dBm 802.11a/54M: 15dBm+/-1dBm 802.11n/HT20-MCS7: 13dBm+/-1dBm 802.11n/HT40-MCS7: 13dBm+/-1dBm 802.11ac/VH20-MCS7: 13dBm+/-1dBm 802.11ac/VH40-MCS8: 12dBm+/-1dBm 802.11ac/VH80-MCS9: 11dBm+/-1dBm
Working Current	250 mA ~300mA
Peak Current	500 mA ~650mA
Size	17mm*17mm*2.4mm
Operating temperature	-40℃~+85℃
Storage temperature	-40℃~+125℃
VBAT	3.3V
VDD_PIO	1.8V/3.3V
Humidity	Operating Humidity 10% to 95% Non-Condensing

Table 1: Specifications

5. Pin Diagram And Description

5.1 Pin Diagram

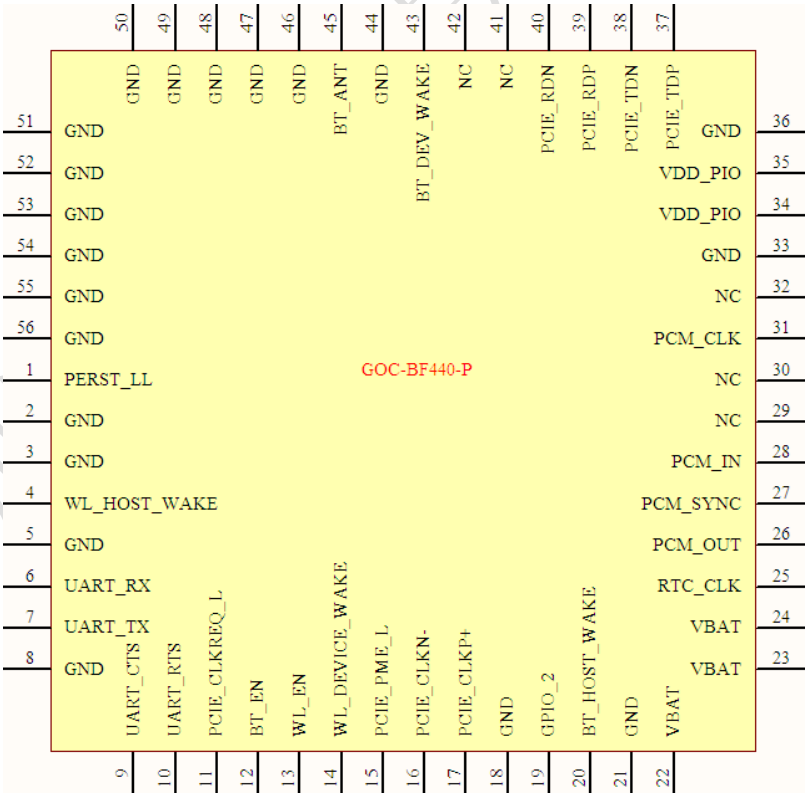


Figure 2: GOC-BF440-P Pin Diagram

5.2 Pin Description

	Pin Name	Type	Description
1	PERST_L	Input(weak internal pull-up resistor)	PCIE Reset.
2	GND	GND	Ground
3	GND	GND	Ground
4	WL_HOST_WAKE	Input/Output	Wlan host wake-up: Signal from the module to the host indicating that the module requires attention.
5	GND	GND	Ground
6	UART_RX	Input	UART serial input
7	UART_TX	Output	UART serial output
8	GND	GND	Ground
9	UART_CTS	Input	UART clear-to-send
10	UART_RTS	Output	UART request-to-send
11	PCIE_CLKREQ_L	Digital Output	PCIe clock request signal which indicates when the REFCLK to the PCIE interface can be gated. 1 = the clock can be gated. 0 = the clock is required.
12	BT_EN	Input	BT enable
13	WL_EN	Input	WL enable
14	WL_DEVICE_WAKE	Input/Output	Wlan device wake-up: Signal from the host to the module indicating that the host requires attention.
15	PCIE_PME_L	Digital Output	PCI power management event output
16	PCIE_CLKN-	Input	PCIe differential clock inputs (negative)
17	PCIE_CLKP+	Input	PCIe differential clock inputs (positive)
18	GND	GND	Ground
19	GPIO_2	Input/Output	GPIO_2
20	BT_HOST_WAKE	Input/Output	BT host wake-up: Signal from the module to the host indicating that the module requires attention.
21	GND	GND	Ground
22	VBAT	POWER	3.3V Supply Voltage
23	VBAT	POWER	3.3V Supply Voltage
24	VBAT	POWER	3.3V Supply Voltage
25	RTC_CLK	Input	External sleep clock input (32.768 kHz)
26	PCM_OUT	Output	PCM data output
27	PCM_SYNC	Input/Output	PCM sync
28	PCM_IN	Input	PCM data input
29	NC	NC	NC
30	NC	NC	NC
31	PCM_CLK	Input/Output	PCM or SLIMbus clock
32	NC	NC	NC
33	GND	GND	Ground

34	VDD_PIO	POWER	1.8V or 3.3V Supply Voltage
35	VDD_PIO	POWER	1.8V or 3.3V Supply Voltage
36	GND	GND	Ground
37	PCIE_TDP	Output	PCIE_TXDP
38	PCIE_TDN	Output	PCIE_TXDN
39	PCIE_RDP	Input	PCIE_RXDP
40	PCIE_RDN	Input	PCIE_RXDN
41	NC	NC	NC
42	NC	NC	NC
43	BT_DEV_WAKE	Input/Output	BT device wake-up: Signal from the host to the module indicating that the host requires attention.
44	GND	GND	Ground
45	BT_ANT	RF	Bluetooth Antenna
46	GND	GND	Ground
47	GND	GND	Ground
48	GND	GND	Ground
49	GND	GND	Ground
50	GND	GND	Ground
51	GND	GND	Ground
52	GND	GND	Ground
53	GND	GND	Ground
54	GND	GND	Ground
55	GND	GND	Ground
56	GND	GND	Ground

Table 2: Pin Description

5.3 PCB Layout Footprint

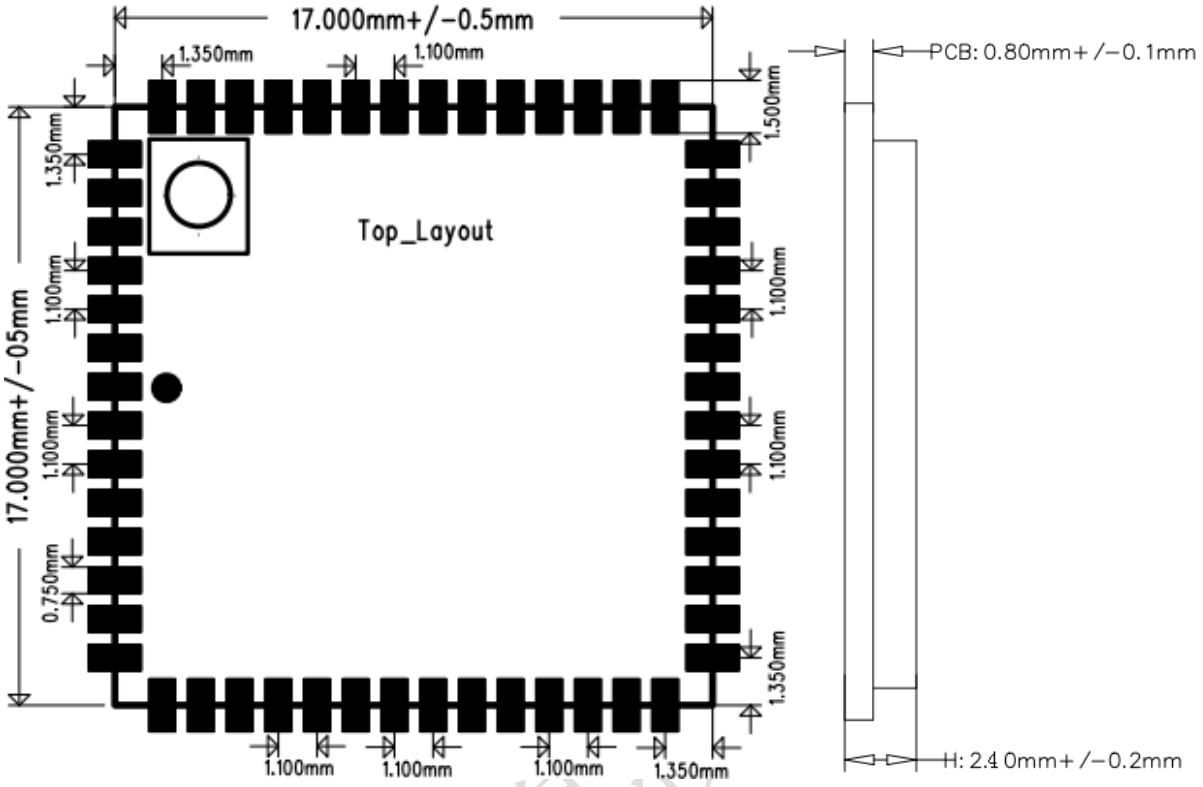


Figure 3: PCB Layout Footprint

6. External LPO_CLK Signal Requirement

Parameter	**LPO Clock**	**Units**
Nominal input frequency	32.768	kHz
Frequency accuracy	±200	ppm
Duty cycle	30–70	%
Input signal amplitude	200–3300	mV, p-p
Signal type	Square wave or sine wave	–
Input impedancel[1]	>100k	Ω
	<5	pF
Clock jitter (during initial start-up)	<10,000	ppm

1. When power is applied or switched off.

Table 3: External LPO_CLK Signal Requirement

7. Echo Cancellation Principle

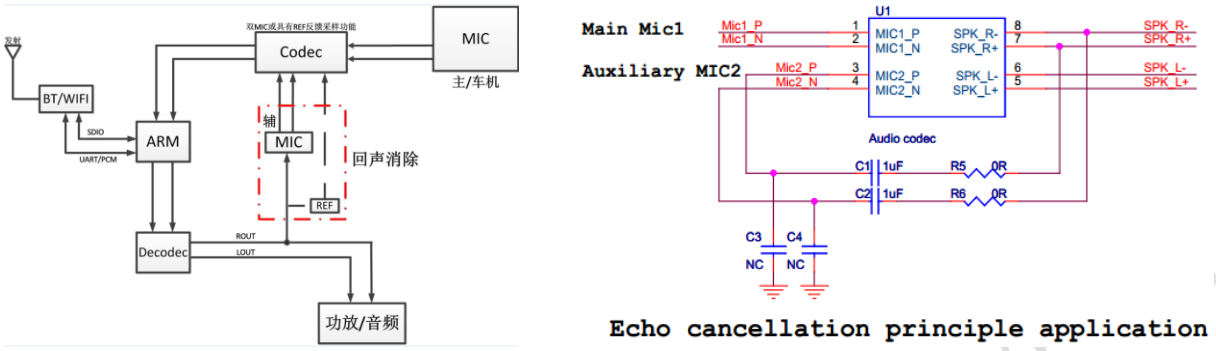


Figure 5: Echo Cancellation Principle

The left picture is a schematic diagram of the echo cancellation principle. After Decodec decoding of the left and right channel sound, after data sampling and master MIC data comparison, echo cancellation can be processed. The right picture is a reference example, which can be designed according to the actual plan. Flying echo cancellation design, priority to use the echo cancellation design of IFLYTEK.

8. Power-Up Sequence and Timing

8.1 Sequencing of Reset and Regulator Control Signals

The GOC-BF440-P has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states. The timing values indicated are minimum required values; longer delays are also acceptable.

NOTE:

1)The module has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 150 ms after VDDC and VDDIO are available before initiating SDIO accesses.

2)VBAT should not rise 10%–90% faster than 40 microseconds. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

8.2 Power on sequence for WLAN ON and BT ON

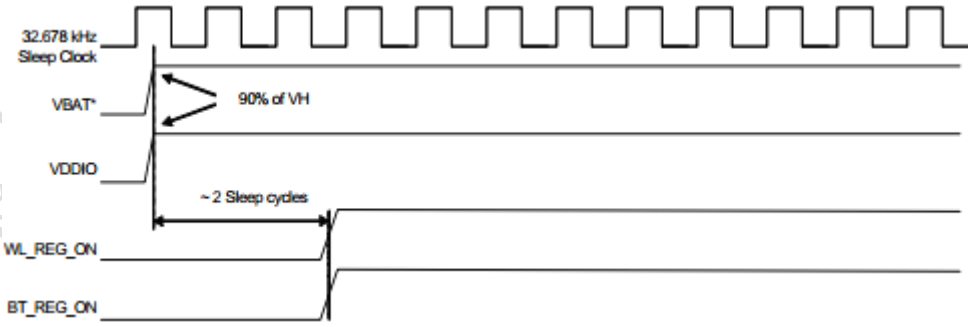


Figure 6: WLAN = ON, Bluetooth = ON

Notes:

1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

8.3 Power OFF Sequence for WLAN OFF and BT OFF

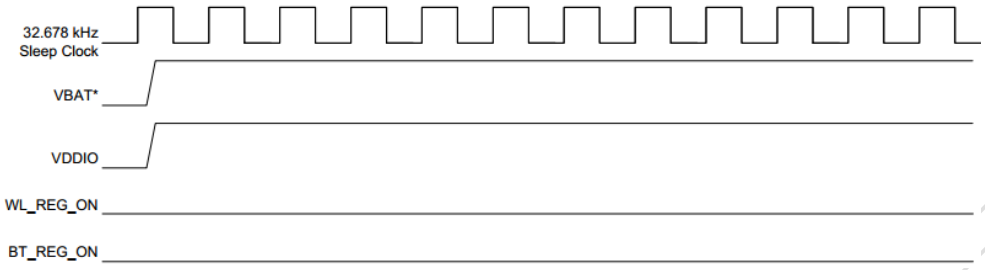


Figure 7: WLAN = OFF, Bluetooth = OFF

Notes:
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

8.4 Power On Sequence for WLAN On and BT OFF

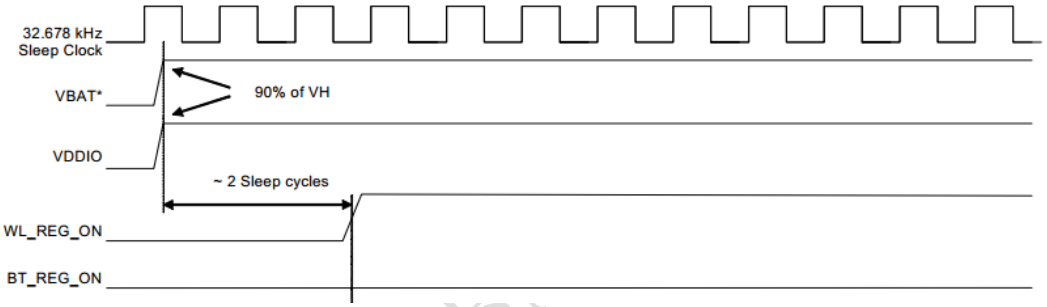


Figure 8: WLAN = ON, Bluetooth = OFF

Notes:
1. VBAT should not rise 10%–90% faster than 40 microseconds.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

8.5 Power On Sequence for WLAN OFF and BT On

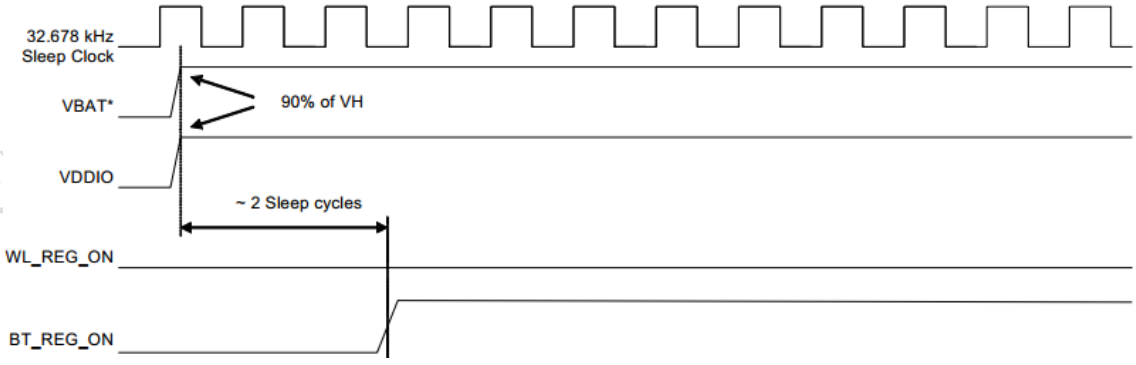


Figure 9: WLAN = OFF, Bluetooth = ON

Notes:
1. VBAT should not rise 10%–90% faster than 40 microseconds.

2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

9. UART Interface

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 4.1 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

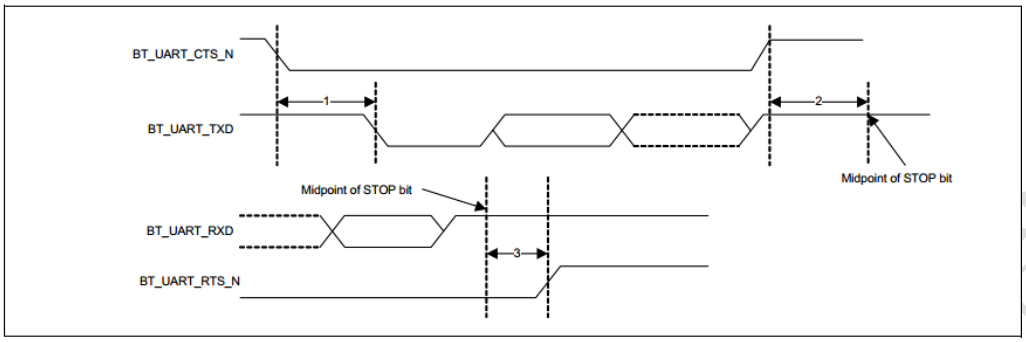
The GOC-BF440-P UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The GOC-BF440-P UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

Table 4: Example of Common Baud Rate

UART Timing



UART Timing Specifications

Ref	Characteristics	Min	Typ	Max	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

10. PCM Interface

The PCM Interface on the GOC-BF440-P can connect to linear PCM Codec devices in master or slave mode. In master mode,the GOC-BF440-P generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the GOC-BF440-P.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Slot Mapping

The GOC-BF440-P supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

Frame Synchronization

The GOC-BF440-P supports both short- and long-frame synchronization in both master and slave modes. In shortframe synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

Data Formatting

The GOC-BF440-P may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the GOC-BF440-P uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

PCM Interface Timing

Short Frame Sync, Master Mode

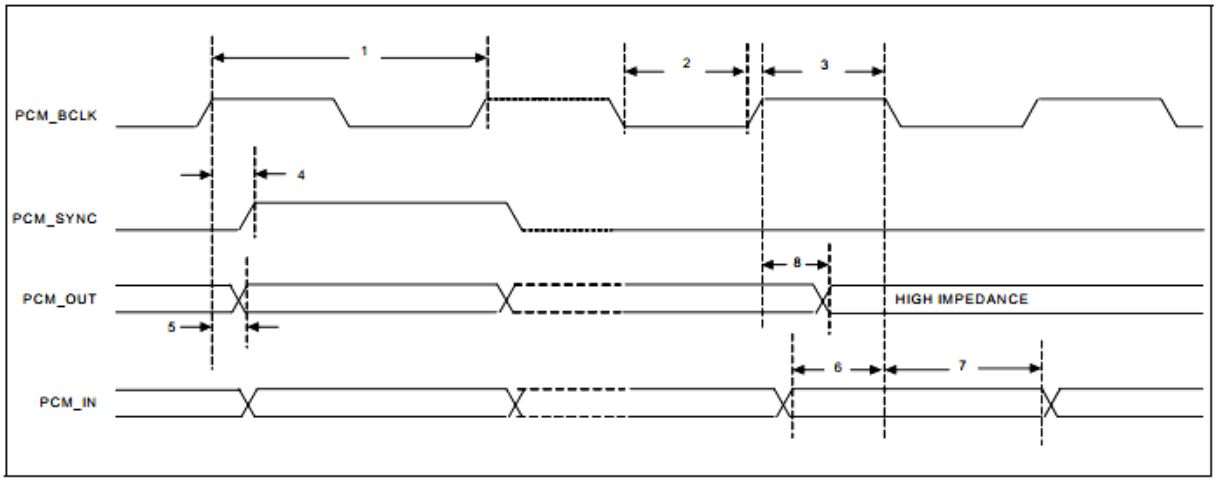


Figure 10: PCM Timing Diagram (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock LOW	41	-	-	ns
3	PCM bit clock HIGH	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

Table 5: PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Short Frame Sync, Slave Mode

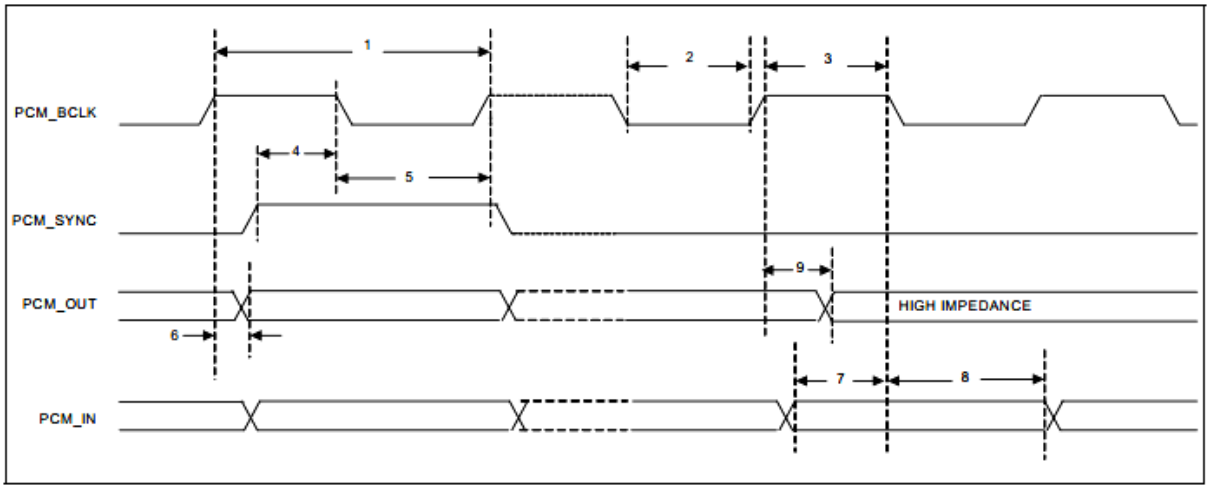


Figure 11: PCM Timing Diagram (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock LOW	41	-	-	ns
3	PCM bit clock HIGH	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

Table 6: PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Long Frame Sync, Master Mode

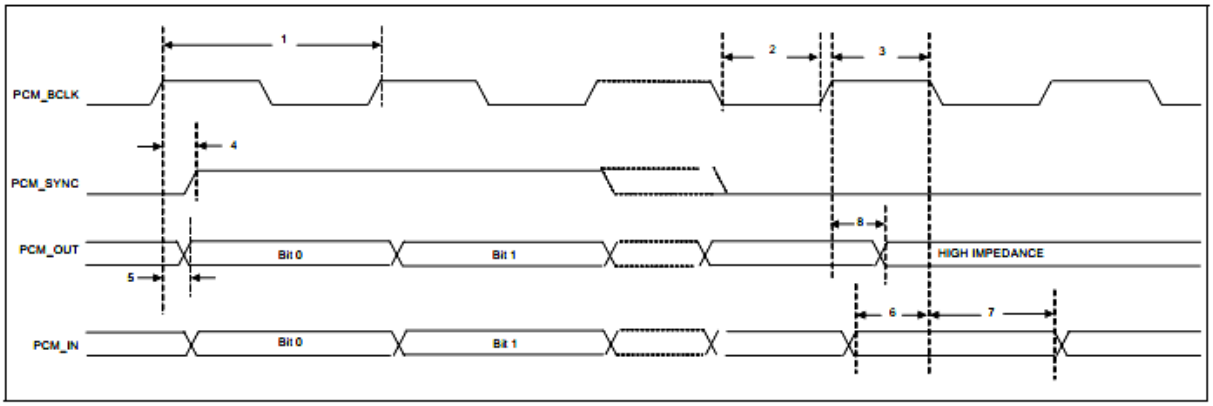


Figure 12: PCM Timing Diagram (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock LOW	41	-	-	ns
3	PCM bit clock HIGH	41	-	-	ns
4	PCM_SYNC delay	0	-	25	ns
5	PCM_OUT delay	0	-	25	ns
6	PCM_IN setup	8	-	-	ns
7	PCM_IN hold	8	-	-	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

Table 7: PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Long Frame Sync, Slave Mode

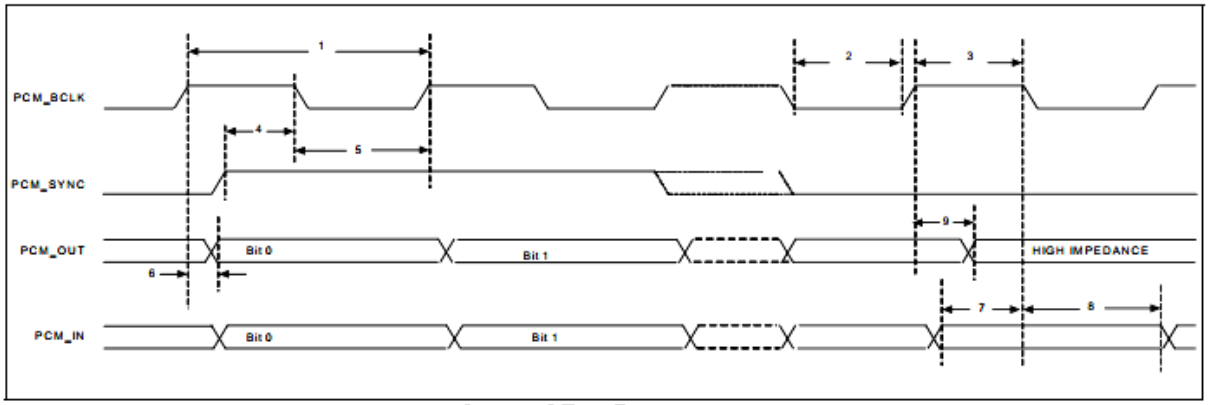


Figure 13: PCM Timing Diagram (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock LOW	41	-	-	ns
3	PCM bit clock HIGH	41	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	0	-	25	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	-	25	ns

Table 8: PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Short Frame Sync, Burst Mode

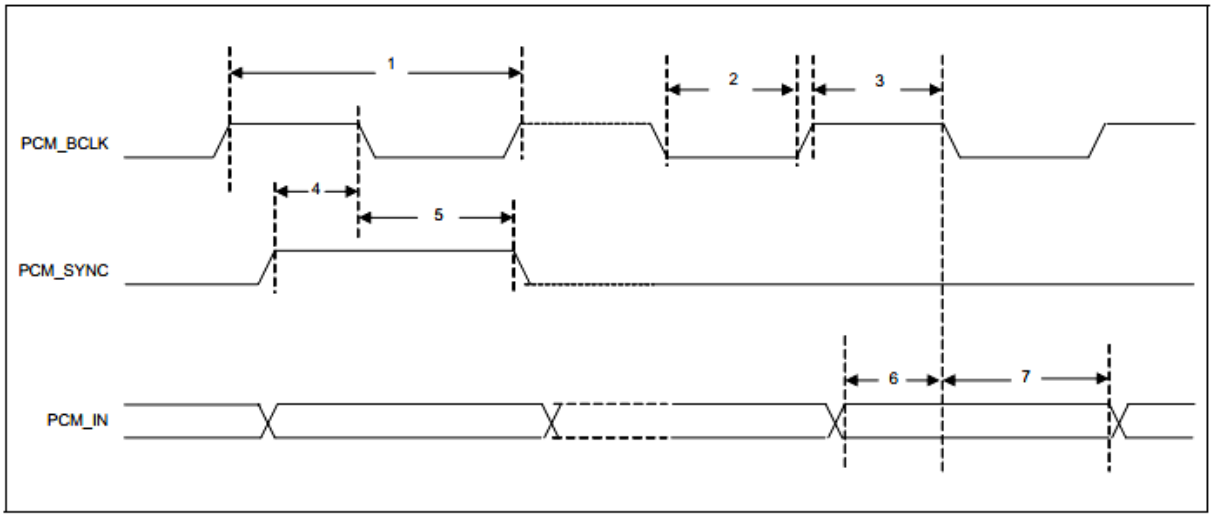


Figure 14: PCM Burst Mode Timing (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock LOW	20.8	-	-	ns
3	PCM bit clock HIGH	20.8	-	-	ns
4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	8	-	-	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns

Table 9: PCM Burst Mode (Receive Only, Short Frame Sync)

Long Frame Sync, Burst Mode

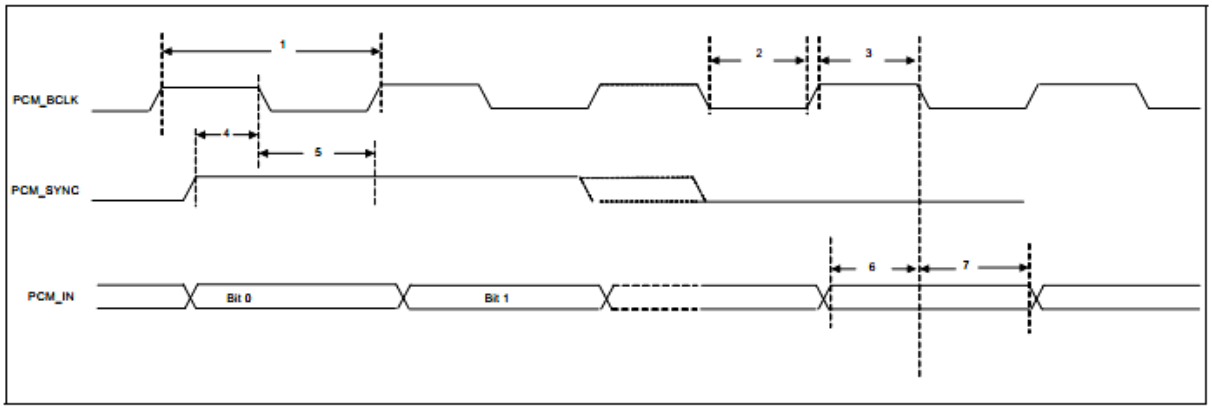


Figure 15: PCM Burst Mode Timing (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock LOW	20.8	-	-	ns
3	PCM bit clock HIGH	20.8	-	-	ns

4	PCM_SYNC setup	8	-	-	ns
5	PCM_SYNC hold	8	-	-	ns
6	PCM_OUT delay	8	-	-	ns
7	PCM_IN setup	8	-	-	ns
8	PCM_IN hold	8	-	-	ns

Table 10: PCM Burst Mode (Receive Only, Long Frame Sync)

11. PCIE Interface

The PCI Express (PCIe) core on the GOC-BF440-P is a high-performance serial I/O interconnect that is protocol compliant and electricallycompatible with the PCI Express Base Specification v2.0. This core contains all the necessary blocks, including logical and electrical
functional subblocks to perform PCIe functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

Organization of the PCIe core is in logical layers: Transaction Layer, Data Link Layer, and Physical Layer, as shown in Figure 16. A configuration or link management block is provided for enumerating the PCIe configuration space and supporting generation and reception of System Management Messages by communicating with PCIe layers.

Each layer is partitioned into dedicated transmit and receive units that allow point-to-point communication between the host and GOC-BF440-P device. The transmit side processes outbound packets while the receive side processes inbound packets. Packets are formed and generated in the Transaction and Data Link Layer for transmission onto the high-speed links and onto the receiving device. A header is added at the beginning to indicate the packet type and any other optional fields.

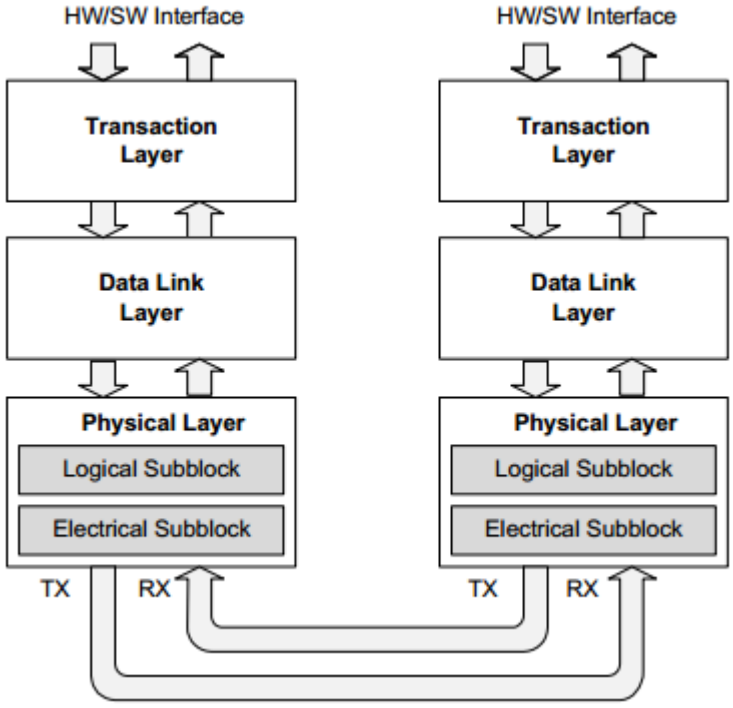


Figure 16: PCI Express Layer Model

11.1 Transaction Layer Interface

The PCIe core employs a packet-based protocol to transfer data between the host and GOC-BF440-P device, delivering new levels of performance and features. The upper layer of the PCIe is the Transaction Layer. The Transaction layer is primarily responsible for assembly and disassembly of Transaction Layer Packets (TLPs). TLP structure contains header, data payload, and End-to-End CRC(ECRC) fields, which are used to communicate transactions, such as read and write requests and other events.

A pipelined full split-transaction protocol is implemented in this layer to maximize efficient communication between devices with creditbased flow control of TLP, which eliminates wasted link bandwidth due to retries.

11.2 Data Link Layer

The data link layer serves as an intermediate stage between the transaction layer and the physical layer. Its primary responsibility is to provide reliable, efficient mechanism for the exchange of TLPs between two directly connected components on the link. Services provided by the data link layer include data exchange, initialization, error detection and correction, and retry services.

Data Link Layer Packets (DLLPs) are generated and consumed by the data link layer. DLLPs are the mechanism used to transfer link management information between data link layers of the two directly connected components on the link, including TLP acknowledgment, power management, and flow control.

11.3 Physical Layer

The physical layer of the PCIe provides a handshake mechanism between the data link layer and the high-speed signaling used for Link data interchange. This layer is divided into the logical and electrical functional subblocks. Both subblocks have dedicated transmit and receive units that allow for point-to-point communication between the host and GOC-BF440-P device. The transmit section prepares outgoing information passed from the data link layer for transmission, and the receiver section identifies and prepares received information before passing it to the data link layer. This process involves link initialization, configuration, scrambler, and data conversion into a specific format.

11.4 Logical Subblock

The logical sub block primary functions are to prepare outgoing data from the data link layer for transmission and identify received data before passing it to the data link layer.

11.5 Scrambler/Descrambler

This PCIE PHY component generates pseudo-random sequence for scrambling of data bytes and the idle sequence. On the transmit side, scrambling is applied to characters prior to the 8b/10b encoding. On the receive side, descrambling is applied to characters after 8b/10b decoding. Scrambling may be disabled in polling and recovery for testing and debugging purposes.

11.6 8B/10B Encoder/Decoder

The PCIE core on the GOC-BF440-P uses an 8b/10b encoder/decoder scheme to provide DC balancing, synchronizing clock and data recovery, and error detection. The transmission code is specified in the ANSI X3.230-1994, clause 11 and in IEEE 802.3z, 36.2.4.

Using this scheme, 8-bit data characters are treated as 3 bits and 5 bits mapped onto a 4-bit code group and a 6-bit code group, respectively. The control bit in conjunction with the data character is used to identify when to encode one of the twelve Special Symbols included in the 8b/10b transmission code. These code groups are concatenated to form a 10-bit symbol, which is then transmitted serially. Special Symbols are used for link management, frame TLPs, and DLLPs, allowing these packets to be quickly identified and easily distinguished.

11.7 Elastic FIFO

An elastic FIFO is implemented in the receiver side to compensate for the differences between the transmit clock domain and the receive clock domain, with worse case clock frequency specified at 600 ppm tolerance. As a result, the transmit and receive clocks can shift one clock every 1666 clocks. In addition, the FIFO adaptively adjusts the elastic level based on the relative frequency difference of the write and read clock. This technique reduces the elastic FIFO size and the average receiver latency by half.

11.8 Electrical Subblock

The high-speed signals utilize the Common Mode Logic (CML) signaling interface with on-chip termination and de-emphasis for bestin-class signal integrity. A de-emphasis technique is employed to reduce the effects of Intersymbol Interference (ISI) due to the interconnect by optimizing voltage and timing margins for worst case channel loss. This results in a maximally open "eye" at the detection point, thereby allowing the receiver to receive data with acceptable Bit-Error Rate (BER).

To further minimize ISI, multiple bits of the same polarity that are output in succession are de-emphasized. Subsequent same bits are reduced by a factor of 3.5 dB in power. This amount is specified by PCIe to allow for maximum interoperability while minimizing the complexity of controlling the de-emphasis values. The high-speed interface requires AC coupling on the transmit side to eliminate the DC common mode voltage from the receiver. The range of AC capacitance allowed is 75 nF to 200 nF.

11.9 Configuration Space

The PCIe function in the GOC-BF440-P implements the configuration space as defined in the PCI Express Base Specification v2.0.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Rated Level	Min	Typical	Max	Remark
VBAT	3.13V	3.3V	4.8V	/
VDD_PIO	3.13V	3.3V	3.47V	/
	1.71V	1.8V	1.89V	/

Table 11: Absolute Maximum Ratings

12.2 Recommended Operating Conditions

Working Condition	Min	Typical	Max
Temperature Range	-40℃	/	+85℃
Storage Temperature	-40℃	/	+125℃
VBAT	3.13V	3.3V	3.47V
VDD_PIO	3.13V	3.3V	3.47V
	1.71V	1.8V	1.89V

Table 12: Recommended Operating Conditions

13. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : ≦260℃

Number of Times : 2 times

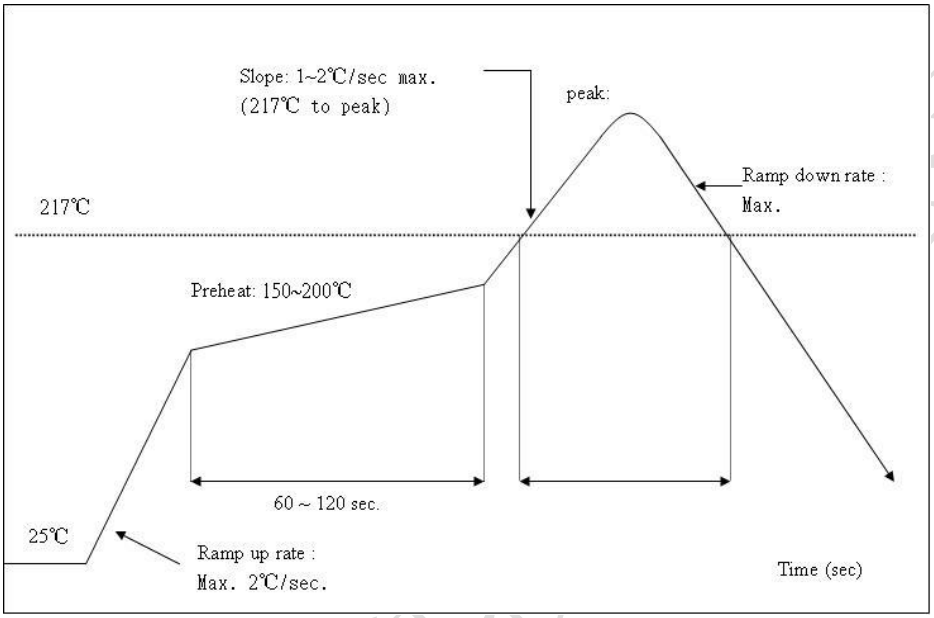


Figure 17: Solder Reflow Profile

14. PCB Layout Recommendation

14.1 Antenna

Antenna trace impedance should be adjusted to 50ohm.The area above(or under)the RF antenna trace should be free from other traces.

14.2 HCI UART Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA

UART_RX UART_TX UART_CTS UART_RTS

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω.

14.3 PCM Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 mA

PCM_SYNC PCM_CLK PCM_OUT PCM_IN

The route length of these signals be less than 15 cm and the line impedance be less than 50Ω.

14.4 Power Trace Lines Layout Guideline

－VBAT Trace Width: 20mil

14.5 Ground Lines Layout Guideline

- A Complete Ground in Ground Layer.
- Add Ground Through Holes to GOC-BF440-P Module Ground Pads
- Decoupling Capacitors close to GOC-BF440-P Module Power and Ground Pads

14. Module Part Number Description

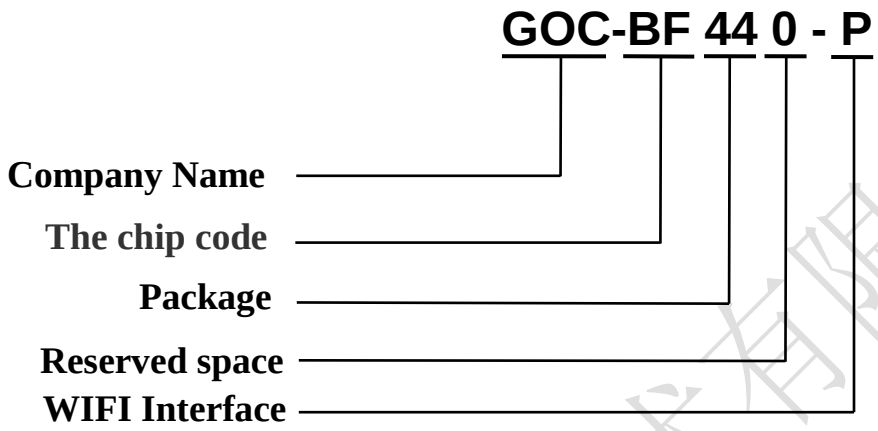


Figure 18: Module Part Number Description

For a list of available options (e.g. package, packing) and orderable part numbers or for further information on any aspect of this device, please go to www.goodocom.com or contact the GOODOCOM Sales Office nearest to you.

15. Ordering Information

Part Number	Description	Remark
GOC-BF440-P	Bluetooth+WIFI Module	

Table 13: Ordering Information

16. Packaging Information

16.1 Net Weight

The module net weight: 1.3g±0.1g

16.2 Package

72pcs module in one tray 2000pcs modules into one pack 4000pcs

Modules One Box Carton size:270mm*275mm*220mm

Tray size:225mm*205mm*7mm

16.3 Storage Requirements

1）Temperature: 22~28℃;

2）Humidity: <70%（ RH）;

Vacuum packed and sealed in good condition to ensure 12 months of welding.

16.4 Humidity Sensitive Characteristic

1） MSL: 3 level

2） Once opened, SMT within 168 hours in the condition of temperature: 22~28℃ and humidity<60%(RH).

3） Handling, storage, and processing should follow IPC/JEDECJ-STD-033